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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,542	09/30/2003	Moo Jin Lee	049128-5127	1841

  

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EXAMINER	
XIAO, KE	

  

ART UNIT	PAPER NUMBER
2629	

  

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07/13/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/673,542

Applicant(s)

LEE ET AL.

Examiner

Ke Xiao

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 09 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 5,6 and 18-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 5,6 and 18-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 5, 6 and 18-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nanno (WO 02/35507) in view of Moon (US 6,480,180).

Regarding **Claim 5**, Nanno teaches a method of supplying a power to a liquid crystal display (Nanno, Fig. 2) comprising the steps of:

taking a power source voltage less than 3.0V from a system (Nanno, Fig. 4 element Vdd 1.8V);

supplying the power source voltage to digital circuit devices including an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal (Nanno, Fig. 2 element 24).

Nanno fails to teach that the interface circuit includes a low voltage differential signal receiver as claimed. Moon teaches a low voltage differential signaling interface which lowers a voltage level of the signals input from the system to thereby reduce the number of signal lines needed to the system and the timing controller (Moon, Fig. 7). It would have been obvious to one of ordinary skill in the art at the time of the invention

to use the LVDS interface device of Moon in the system of Nanno in order to reduce the number of transmission lines and eliminate EMI problems (Moon, Col. 2 lines 43-47).

Regarding **Claim 6**, Nanno further teaches the step of raising or reducing the power source voltage from the system to generate voltage to be supplied to the liquid crystal panel (Nanno, Fig. 4 element 24).

Regarding **Claim 18**, Nanno teaches a method of supplying a power to a liquid crystal display (Nanno, Fig. 2) comprising the steps of:

a system for generating a power voltage under 3.0V (Nanno, Fig. 4 element Vdd 1.8V);

s digital circuit devices including an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit used to process the digital signal by taking the power voltage (Nanno, Fig. 2 element 24).

Nanno fails to teach that the interface circuit includes a low voltage differential signal receiver as claimed. Moon teaches a low voltage differential signaling interface which lowers a voltage level of the signals input from the system to thereby reduce the number of signal lines needed to the system and the timing controller (Moon, Fig. 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the LVDS interface device of Moon in the system of Nanno in order to reduce the number of transmission lines and eliminate EMI problems (Moon, Col. 2 lines 43-47).

Regarding **Claim 19**, Nanno further teaches a DC-DC converter for raising or reducing the power source voltage to generate the raised or the reduced voltage to be supplied to the liquid crystal panel (Nanno, Fig. 4 element 24).

Regarding **Claim 20**, Nanno further teaches that the digital circuit device includes:

- an interface circuit for receiving a synchronous signal, a clock signal and digital video data from the system (Nanno, Figs. 11 and 12);

- a data driving circuit for supplying the digital video data to the liquid crystal panel (Nanno, Fig. 2 source driver element 22c);

- a gate driving circuit for supplying a scan pulse to the liquid crystal panel (Nanno, Fig. 2 gate driver element 21c); and

- a timing controller for controlling the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the interface circuit (Nanno inherently teaches a timing controller because of the clock and sync signals used by the drivers).

### ***Response to Arguments***

Applicant's arguments with respect to Claims 5, 6 and 18-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571) 272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 26<sup>th</sup>, 2007 - kx -

  
SUMATI LEFKOWITZ  
SUPERVISORY PATENT EXAMINER